an impurity region including a second impurity having an opposite conductive type to the first impurity and being formed under the channel forming region,

wherein a concentration of the second impurity in the channel forming region is from 1/100 to 1/10 of that in the impurity region,

wherein the second impurity is introduced from a direction of the < 110 > axis with respect to the single crystal semiconductor substrate, so that the second impurity is introduced from a perpendicular direction to a plane having the smallest atomic density of the single crystal semiconductor substrate,

wherein the concentration of the second impurity in the impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3,

wherein the concentration of the second impurity in the channel forming region is in a range of 1×10^{16} to 1×10^{17} atoms/cm^3,

wherein the second impurity is introduced with a diagonal direction in a range of $45° \pm 3°$ with respect to a surface of the single crystal semiconductor substrate.

27. (Amended) A device according to claim 1, wherein the impurity region is formed at a depth in a range of 20 to 150 nm from a surface of the single crystal semiconductor substrate.

28. (Amended) A device according to claim 1, wherein the single crystal semiconductor substrate is a single silicon substrate.

29. (Amended) A semiconductor device comprising a plurality of MOSFETs formed in a single crystal semiconductor substrate,

each of the plurality of MOSFETs comprising:

a source region and a drain region each including a first impurity;

a channel forming region being formed between the source region and the drain region;

an impurity region including a second impurity having an opposite conductive type to the first impurity and being formed under the channel forming region;

a pair of LDD regions, wherein one of the pair of LDD regions is formed between the source region and the channel forming region while the other of the pair of LDD regions is formed between the channel forming region and the drain region,

wherein a concentration of the second impurity in the channel forming region is from 1/100 to 1/10 of that in the impurity region,

wherein the second impurity is introduced from a direction of the < 110 > axis with respect to the single crystal semiconductor substrate, so that the second impurity is introduced from a perpendicular direction to a plane having the smallest atomic density of the single crystal semiconductor substrate,

wherein the concentration of the second impurity in the impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3,

wherein the second concentration of the impurity in the channel forming region is in a range of 1×10^{16} to 1×10^{17} atoms/cm^3,

wherein the second impurity is introduced with a diagonal direction in a range of $45° \pm 3°$ with respect to a surface of the single crystalline semiconductor substrate.

34. (Amended) A device according to claim 29, wherein the impurity region is formed

at a depth in a range of 20 to 150 nm from a surface of the single crystal semiconductor substrate.

42. (Amended) A semiconductor device comprising at least a CMOS circuit including an n-channel MOSFET and a p-channel MOSFET each being formed in a single crystal semiconductor substrate;

said n-channel MOSFET comprising:

a first source region and a first drain region each comprising a first n-type impurity;

a first channel forming region being formed between the first source region and the first drain region;

a first impurity region including a first p-type impurity and being formed under the first channel forming region;

said p-channel MOSFET comprising:

a second source region and a second drain region each comprising a second p-type impurity;

a second channel forming region being formed between the second source region and the second drain region;

a second impurity region including a second n-type impurity and being formed under the second channel forming region,

wherein each of the first p-type and the second n-type impurities is introduced from a direction of the < 110 > axis with respect to the single crystal semiconductor substrate, so that each of the first p-type and the second n-type impurities is introduced from a perpendicular

direction to a plan having the smallest atomic density of the single crystal semiconductor substrate,

wherein a concentration of the first p-type impurity in the first impurity region is in a range of 1 x 10^{18} to 1 x 10^{19} atoms/cm^3,

wherein a concentration of the first p-type impurity in the first channel forming region is in a range of 1 x 10^{16} to 1 x 10^{17} atoms/cm^3

wherein a concentration of the second n-type impurity in the second impurity region is in a range of 1 x 10^{18} to 1 x 10^{19} atoms/cm^3,

wherein a concentration of the second n-type impurity in the second channel forming region is in a range of 1 x 10^{16} to 1 x 10^{17} atoms/cm^3,

wherein each of the first p-type and the second n-type impurities is introduced with a diagonal direction in a range of 45°±3° with respect to a surface of the single crystal semiconductor substrate.

48. (Amended) A device according to claim 42, wherein each of the first and second impurity regions is formed at a depth in a range of 20 to 150 nm from a surface of the single crystal semiconductor substrate.